

FORM PTO-1449 U.S. Department of Commerce (Rev. 4/92) Patent and Trademark Office INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	ATTY. DOCKET NO. 501.25958CV7	SERIAL NO. Not yet assigned
	APPLICANT HOTTA, et al	
	FILING DATE November 6, 2003	GROUP 2185

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROP
DmB	4 6 6 1 7 2 1	4(87)	Ushiku	307	269	8/21/87
	4 7 6 1 5 6 5	8/88	Kannagundla	307	243	
	4 9 5 8 0 9 2	9/90	Tanaka	307	480	
	5 4 5 1 8 9 2	9/95	Bailey	327	113	10/3/94
	4 6 8 9 5 8 1	8/87	Talbot	331	1A	7/31/85
	3 9 4 0 5 5 8	2/76	Gabbard	375	356	
	4 8 2 3 2 6 2	4/89	Calle	395	550	6/26/87
	4 6 9 2 9 3 2	9/87	Denhez	375	356	2/6/86
	4 6 8 0 7 7 9	7/87	Wakerly	375	356	1/14/87
	4 5 1 9 0 7 1	5/85	Miller	370	105.3	
DmB	4 6 3 9 8 5 6	1/87	Hristich	395	575	11/4/87

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT
						YES
DmB	0 1 1 3 5 1 6	7/84	European			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DmB	Kazuo Kato, et al, "A Low-Power 128 MHZ VCO for Monolithic PLL IC's" IEEE Journal of Solid State Circuits, 1988, vol. 23, No. 2, pp. 474-479.
DmB	Deog-Kyoun-Jeong, "Design of PLL-Based Clock Generation Circuits", IEEE Journal of Solid State Circuits, 1987, vol. SC-22, No. 2, pp. 255-261.
DmB	"A Synchronous Approach for Clocking VLSI Systems", IEEE Journal of Solid State Circuits, February 1982, SC-17, No. 1, pp. 51-56.

EXAMINER *Dennis M. Butler* DATE CONSIDERED *11-28-05*

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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DMB	5 0 9 5 4 2 5	3/92	Hesse	395	550	1/9/85
	4 8 9 0 2 2 2	12/89	Kirk	395	550	12/17/89
	4 5 9 0 4 3 9	5/89	Goggin	331	60	5/7/84
	4 8 4 7 5 1 6	7/89	Fujita	307	269	11/23/89
	3 7 5 8 7 2 0	9/73	Dinn	307	269	
	3 8 2 9 7 9 0	8/74	Macrander	331	61	
	4 8 9 3 2 7 1	1/90	Davis	364	900	11/7/83
	4 4 6 8 6 3 4	8/84	Takagi	331	60	
	3 9 6 1 2 6 9	6/76	Alvarez	331	60	
	4 5 2 1 8 9 3	6/85	Bellman	331	60	
DMB	4 9 0 6 9 4 4	3/90	Frerking	31	1A	8/11/88

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	ABSTRACT
					YES

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DMB	"A 130 k-Gate CMOS Mainframe Chip Sets", ISSCC, Session VIII, pp. 86-87.
DMB	"A ISMIPS 326 Microprocessors", ISSCC, Session II, 1987, pp. 26-27.
DMB	"A Low-Power 128-MHz VCO for Monolithic PLL1C's", K. Kato, IEEE Journal of Solid-State Circuits, vol. 23, April 1988, pp. 474-479.

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	4	8	2	9	5	4	5						
DmB	4	8	2	9	5	4	5	5/89	Guzik	331	1A	8/25/88	
	4	8	6	2	1	0	4	8/89	Muratani	331	1A	4/6/88	
	4	8	6	4	2	5	3	9/89	Zwack	331	1A	9/21/88	
	4	7	7	9	0	0	8	10/88	Kessels	331	1A	10/11/88	
	4	6	7	3	8	9	1	6/87	Remy	331	2		
	4	4	8	6	8	5	0	12/84	Hyatt	364	747		
	4	6	3	0	1	9	3	12/86	Kris	364	200	9/23/88	
	4	6	4	4	4	9	8	2/87	Bedard	364	900	9/26/88	
	4	5	0	4	7	4	5	3/85	Spence	307	270		
	4	7	5	4	1	6	4	6/88	Flora	307	269	6/30/88	
DmB	4	6	7	7	3	9	4	6/87	Vollmer	331	1A	6/21/88	

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	4	7	7	4	6	8	6						
DMB	4	7	7	4	6	8	6	9/88	McClary	364	736	3/21/86	
↓	4	0	7	9	3	7	1	3/78	Shimamura	341	61		
	4	7	1	9	5	9	3	1/88	Threewitt et al	713	500		
	4	4	9	4	1	9	6	1/85	Greet	64	236.2		
	4	1	0	1	9	6	9	7/78	Lawson et al	713	600		
DMB	5	1	3	3	0	6	4	7/92	Hotta et al	395	550		

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